

(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(11) 59-191935 (A) (43) 31 10 1984 (19) JP

(21) Appl. No. 58-65459 (22) 15.4.1983

(71) HITACHI SEISAKUSHO K.K. (72) TSUNEO ITOU

(51) Int. Cl. H03K19/00

PURPOSE: To perform aging simply and with high efficiency by having conduction of a semiconductor switch element when the power supply voltage is higher than the working voltage and then connecting an input terminal to a high or low logical potential.

CONSTITUTION: The power supply voltage V_{dd} is clamped at a fixed level by a constant voltage diode D_2 and applied to a common gate of CMOS inverters Q_{p2} and Q_{n2} . The threshold value V_T of inverters Q_{p2} and Q_{n2} is increased in response to the voltage V_{dd} . Thus the value V_T is set higher the range of the normal working power supply voltage and at the same time lower than the power supply voltage which is applied for aging. Then switching elements $Q_1 \sim Q_n$ are electrically conducted and driven via a CMOS buffer Ib when the power supply voltage exceeds the value V_T . An input terminal is set at the logical potential of one side. When the aging is over, a normal operation is reset since the generation of control voltage C is impossible.

